

## CLAIMS

We claim:

- 1                   1.     A method, comprising:  
2     partitioning a cache array dynamically based upon requests for memory  
3     from an integrated device having a plurality of processors.
- 1                   2.     The method as claimed in claim 1, further comprising  
2     subdividing one or more ways within the cache array.
- 1                   3.     The method as claimed in claim 1, further comprising  
2     subdividing one or more sets within the cache array.
- 1                   4.     The method as claimed in claim 1, further comprising using  
2     a single least recently used array to replace ways.
- 1                   5.     The method as claimed in claim 1, further comprising  
2     applying a multiple pseudo least recently used update based on an entry  
3     hit.
- 1                   6.     The method as claimed in claim 1, further comprising  
2     partitioning dynamically the cache array into a direct-mapped cache.
- 1                   7.     A device comprising:

2 a cache memory array dynamically partitioned when multiple memory  
3 requests are received from an integrated device having a plurality of  
4 processors.

1 8. The device as claimed in claim 7 further comprising:  
2 an integrated device having a plurality of processors connected to the  
3 cache memory array.

1 9. The device as claimed in claim 7 further comprising a main  
2 memory device connected to the cache memory array.

1 10. The device as claimed in claim 8 wherein the integrated  
2 device includes a graphics processor and a central processing unit.

1 11. A computer-readable medium having stored thereon a  
2 plurality of instructions, said plurality of instructions when executed by a  
3 computer, cause said computer to perform the method of:  
4 partitioning a cache array dynamically based upon requests for memory  
5 from an integrated device having a plurality of processors.

1 12. The computer-readable medium of claim 11 having stored  
2 thereon additional instructions, said additional instructions when executed  
3 by a computer, cause said computer to further perform the method of  
4 subdividing one or more ways within the cache array.

1           13.    The computer-readable medium of claim 11 having stored  
2           thereon additional instructions, said additional instructions when executed  
3           by a computer, cause said computer to further perform the method of  
4           subdividing one or more sets within the cache array.

1           14.    The computer-readable medium of claim 11 having stored  
2           thereon-additional instructions, said additional instructions when executed  
3           by a computer, cause said computer to further perform the method of  
4           using a single least recently used array to replace ways.

1           15.    The computer-readable medium of claim 11 having stored  
2           thereon-additional instructions, said additional instructions when executed  
3           by a computer, cause said computer to further perform the method of  
4           applying a multiple pseudo least recently used update based on an entry  
5           hit.

1           16.    The computer-readable medium of claim 11 having stored  
2           thereon-additional instructions, said additional instructions when executed  
3           by a computer, cause said computer to further perform the method of  
4           partitioning dynamically the cache array into a direct-mapped cache.

1           17.    A method, comprising:  
2           converting an N-way set associative cache dynamically into a direct  
3           mapped cache; including  
4           removing M least significant bits from a tag address, and

5 adding the M least significant bits to M most significant bits of a set  
6 address of the direct-mapped cache.

1 18. The method of claim 17, wherein N equals 2 to the power M.

1 19. A method, comprising:  
2 converting an N-way set associative cache dynamically into a Z x N-way  
3 set associative cache; including  
4 providing Y+1 virtual copies of a pseudo-LRU array for the N-way set  
5 associative cache, wherein the pseudo-LRU array is not replicated,  
6 and  
7 selecting a virtual copy with Y most significant bits of a set address for  
8 the N-way set associative cache.

1 20. The method of claim 19, wherein Z is 2 to the power Y,  
2 where Y is greater than or equal to 1.

1 21. The method of claim 19, wherein the Y most significant bits  
2 of the set address for the N-way set associative cache become the Y least  
3 significant bits of the tag address for the Z x N-way set associative cache.